REMARKS

I. Introduction

Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested. In response to the Office Action mailed on December 18, 2003, Applicants have amended claims 1 and 2, cancelled claim 13, without prejudice, and added new claims 14 and 15. No new matter has been added.

For the reasons set forth below, Applicants respectfully submit that all pending claims are in condition for allowance.

II. The Rejection Of the Claims in view of Hoge and "IBM"

Claims 1-13 were rejected under 35 U.S.C. § 103 as being unpatentable over USP No. 5,930,158 to Hoge in view of IBM ESA/390 Principles of Operation (hereinafter the IBM reference).

Assuming *arguendo* that the publication date of the IBM reference renders the IBM reference valid prior art to the instant application, Applicants respectfully submit that the pending claims are patentable over Hoge in view of the IBM reference for at least the following reasons.

As recited by the independent claims 1 and 2, the present invention recites an execution control instruction comprising an "**instruction-specifying field containing, in binary code, the number of instructions to be executed**". In other words, the system of the present invention decides how many instructions to be nullified by directly judging the instruction-specifying field.

Turning to the cited prior art reference, the X operated address in Hoge is an address of the General Purpose Register memory (*see*, e.g., col. 4, line 25-27). In particular, the number of

instructions to be nullified in Hoge (count) **is not contained** in the instruction-specifying field but in the General Purposes Register addressed by the X operand address. It is acknowledged in the pending rejection that Hoge does not disclose a condition field containing, in binary code, an execution condition. The IBM reference is relied upon as curing this defect of Hoge. Specifically, as set forth in paragraph 3 of the Office Action, the "Branch On Condition" section of the IBM reference is relied on as curing the foregoing defect.

However, the "Branch On Condition" instruction disclosed by the IBM reference is merely a conditional branch instruction. In other words, if the condition is met, then the branch is set. Likewise, if the condition is not met, then the branch is not set. In contrast to the claimed invention, the Branch On Condition instruction of the IBM reference does not include an instruction-specifying field, much less an instruction-specifying field indicating the number of instructions to be nullified. Indeed, one of the express objectives of the present invention is to reduced the issuance of conditional branch instructions (*see*, e.g., page 1 lines 3-25), such as disclosed by the IBM reference, because conditional branch instructions cause branch hazard (*see*, e.g., page 1 lines 7-12).

It is again noted that an object of the present invention is controlling the conditional execution of as many succeeding instructions as possible using an execution control instruction of ***a short word length*** to suppress the branch hazard in an information processor for processing the instructions by pipelining (*see*, e.g., page 3 of the specification, lines 2-6). Turning to the prior art, if an address of General Purpose Register memory is utilized to specify the number of instructions to be nullified, the necessary instruction word length becomes longer because the allocated bit length must be long enough to designate the General Purpose Register memory.

Based on the foregoing, it is respectfully submitted that, at a minimum, both Hoge and the IBM reference fail to disclose an instruction set having an execution control instruction comprising an "instruction-specifying field containing the number of instructions to be nullified."

Thus, as each and every limitation must be disclosed or suggested by the prior art references in order to establish a *prima facie* case of obviousness (see, MPEP §2143.03), and the combination of Hoge and the IBM reference fail to do so, it is respectfully submitted that claims 1 and 2 are patentable over Hoge and the IBM reference, taken alone or in combination with one another.

III. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 1 and 2 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

It is further noted that Applicants respectfully submit that new claims 14 and 15 recite additional subject matter which is believed to provide an additional basis for patentability over Hoge and the IBM reference.

With regard to claims 14 and 15, these claims recite that the means for deciding whether or not the execution control instruction is satisfied includes comparing the execution condition field to control flags which are determined based on the multiple flags, where the bit number of the execution condition and the control flags are N which is equal to or more than 2. In other words, the system of the present invention judges whether the execution condition is satisfied or not by comparing the N bit control flags to the N bit execution condition which is contained in the condition field itself. Therefore, if the condition fields is N bits, the processor of the present invention is capable of expressing 2^N kinds of conditions. For example, if the present invention utilizes 2-bit as the execution condition, the number of execution condition is thereby 4, and the number of execution conditions may be increased by increasing the bit number of the condition fields (*see*, e.g., page 8, lines 21-23).

In contrast, the condition codes of "IBM" are used to select the corresponding mask bit. If the mask bit selected by the condition code is one, the branch is set (*see*, the IBM reference, page 7-17, right column). In other words, the condition code merely selects the mask bit and the processor judges whether the mask bit is one or zero. The IBM reference appears completely silent as to comparing the N bit control flags to the N bit execution condition which is contained in the condition field itself. Further, the four condition codes of the IBM reference correspond, from left to right, with four bits of the mask. As such, the IBM reference uses 4-bit as the condition field and only expresses 4 kinds of conditions. As discussed above, the present invention controls the conditional execution of as many succeeding instruction as possible using

an execution control instruction of a short word length to suppress the branch hazard in an information processor for processing the instructions by pipelining (see, e.g., page 3 of the specification, lines 2-5). Therefore, for at least these reasons, it is respectfully submitted that claims 14 and 15 are patentably distinct over the prior arts.

IV. Request For Notice of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, and indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

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Date: May 17, 2004